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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/675,841	09/30/2003	Peter B. Criswell	RA5635	6910

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EXAMINER	
DARE, RYAN A	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 04/20/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/675,841	CRISWELL, PETER B.	
	Examiner	Art Unit	
	Ryan Dare	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 February 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4 and 6-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4 and 6-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 September 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. The amendments made to the specification on 2/1/2006 are approved, and the objections to the specification are withdrawn.

Response to Arguments

2. Applicant's arguments with respect to claims 1-4 and 6-37 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-4 and 6-37 are rejected under 35 U.S.C. 102(b) as being anticipated by Lewis et al., US Patent 4,201,337.

1. With respect to claim 1, Lewis et al. teach a control system, comprising:

a storage device to store data signals and a mode designator, the mode designator to select a first or second mode of operation, in the Abstract, where the first mode is the byte parity mode and the second mode is the ECC mode.

a circuit coupled to the storage device to receive as control signals predetermined ones of the data signals, the control signals to control operations of the circuit when the circuit is operating in the first mode, in col. 1, lines 37-41; and

Error Correction Code (ECC) logic coupled to the storage device to interpret the predetermined ones of the data signals as ECC check bits to detect errors in the data signals when the circuit is operating in the second mode, in the Abstract (ECC mode).

2. With respect to claim 2, Lewis et al. teach the system of Claim 1, wherein the storage device is a memory having multiple addressable storage locations, each storing a different respective set of data signals, in fig. 1, main memory 14.

3. With respect to claim 3, Lewis et al. teach the system of Claim 2, wherein each of the addressable storage locations includes circuits to store a respective mode designator to control whether the circuit operates in the first or the second mode after the data signals stored at the addressable storage location are read from the memory, in col. 3, lines 22-28.

4. With respect to claim 4, Lewis et al. teach the system of Claim 3, wherein the circuit includes branch logic to utilize the predetermined ones of the data signals stored at an addressable storage location to generate a next address for addressing the memory if the mode designator stored at the addressable storage location indicates the circuit will operate in the first mode, in col. 2, line 66 through col. 3, line 8. The Control Store 18 controls the sequencing of the instructions read from memory (i.e. branching).

5. With respect to claim 6, Lewis et al. teach the system of Claim 1, wherein the circuit includes logic to provide one or more functions of an instruction processor, in col. 2, line 68 through col. 3, line 2.

6. With respect to claim 7, Lewis et al. teach the system of Claim 1, and further including a programmable storage device coupled to the circuit to select the predetermined ones of the data signals, in fig. 1, Control Store 18.

7. With respect to claim 8, Lewis et al. teach the system of Claim 1, and further including at least one parity circuit coupled to the storage device to determine whether a parity error occurred on any of a predetermined set of the data signals, in col. 4, lines 16-18.

8. With respect to claim 9, Lewis et al. teach the system of Claim 8, wherein the at least one parity circuit includes a circuit to determine whether a parity error occurred on the predetermined set of the data signals when the circuit is operating in the second mode, in col. 4, lines 16-18. The second mode is byte parity mode.

9. With respect to claim 10, Lewis et al. teach the system of Claim 1, wherein the ECC logic is coupled to ECC complement logic to correct errors in the data signals that are detected by the ECC logic when operating in the second mode, in col. 1, lines 48-59.

10. With respect to claim 11, Lewis et al. teach the system of Claim 10, and further including logic coupled to the ECC complement logic to provide data signals to the circuit for use as control signals after any errors detected by the ECC logic have been corrected, in col. 1, lines 34-42.

11. With respect to claims 12-13 and 16-24, these claims describe a method that corresponds to the system as claimed in claims 1-4 and 6-11, and is therefore rejected using similar logic.

12. With respect to claim 14, Lewis et al. teach the method of Claim 13, wherein the storage device is a memory, and wherein the first and second data signals are stored at a same addressable location within the memory, in col. 3, lines 29-40.

13. With respect to claim 15, Lewis et al. teach the method of Claim 14, wherein multiple memory addresses each stores different respective first and second data signals, in col. 3, lines 29-40.

14. With respect to claim 25, Lewis et al. teach the method of Claim 24, and further including:

servicing any error detected by the ECC signals at a time that is optimal for the digital system, in col. 3, lines 35-37 where the ECC bits are stored in the memory for use later; and

servicing any error detected using the parity bits substantially immediately, in col. 3, lines 38-40.

15. With respect to claims 26-37, these claims describe a system that corresponds to various aspects of the system claimed in claims 1-4 and the method claimed in claims 12-25 and is therefore rejected using similar logic.

Conclusion

16. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

17. The prior art made of record on form PTO-892 and not relied upon is considered pertinent to applicant's disclosure. Applicant is required under 37 C.F.R. § 1.111(c) to consider these references fully when responding to this action. The documents cited therein teach similar control systems.

18. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ryan Dare whose telephone number is (571)272-4069. The examiner can normally be reached on Mon-Fri 9:30-6.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571)272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ryan A. Dare
April 17, 2006

MATTHEW KIM
SUPERVISORY PATENT EXAMINER
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